The host/PCI/cache bridge or chipset **106** interfaces to a local expansion bus or system bus **120**. In the preferred embodiment, the local expansion bus **120** is the peripheral component interconnect (PCI) bus **120** or other type of system bus such as a dedicated multimedia or real-time bus. Various types of devices may be connected to the PCI bus **120**. Expansion bus bridge logic **1** and an expansion bus (both not shown) may also be coupled to the PCI bus **120**, as described above.

One or more multimedia devices or multimedia devices **902–910** are coupled to the PCI bus **120**. In the embodiment shown, a CD-ROM **902**, a Video/Graphics card **904**, an Audio card **906**, a telephony card **908**, and an MPEG decoder card **910** may be coupled to the PCI bus **120**. Various other types of peripherals may be connected to the bus **120**, as desired.

Each of the multimedia devices **902–910** includes a dedicated memory data channel **912–920**, respectively, which connects to the memory controller **934** in the chipset logic **106**. Each of the memory data channels is preferably a high speed serial bus, such as the Philips I^2C serial bus from Philips Corp., or a 4 bit, 8 bit bus, or 16 bit bus. Each of the multimedia devices **902–910** uses its dedicated memory data channel **912–920** to perform data accesses and transfers directly to the main memory **110**, bypassing PCI bus arbitration and PCI bus cycles. The dedicated memory channels may also be coupled directly to the main memory **110** instead of to the memory controller **934**.

The multimedia devices **902–910** each include bus interface circuitry **940** which includes standard PCI interface circuitry for communicating on the PCI bus **120**. The interface circuitry **940** in each of the multimedia devices **902–910** also includes interface logic for interfacing to the respective dedicated memory data channel **912–920**. The multimedia devices **902–910** use the PCI bus **120** to communicate data between the respective devices, and each uses its respective channel for main memory accesses.

The multimedia devices **902–910** may be any of various types of input/output devices, including multimedia devices and communication devices, as described above. The multimedia devices **902–910** are preferably similar to the multimedia devices **902–910** described above, except that the interface logic in the multimedia devices **902–910** each include memory data channel interface logic, as described below. As described above, the multimedia devices **902–910** may comprise video accelerator or graphics accelerator cards, video playback cards, MPEG decoder cards, sound cards, network interface cards, SCSI adapters for interfacing to various input/output devices, such as CD-ROMS and tape drives, or other devices as desired.

Thus, the multimedia devices **902–910** communicate with each other via the PCI bus **120** and also communicate with the CPU **102** and main memory **110** via the PCI bus **120**, as is well known in the art.

The multimedia devices **902–910** also each communicate data to and from the main memory **110** using the device's respective dedicated memory data channel. The multimedia devices **902–910** preferably each use its dedicated memory data channel for addressing, control, status and handshaking signals, as well as for data communications. Thus the devices **902–910** do not utilize any PCI bus cycles when communicating over their respective memory data channel. Alternatively, the multimedia devices **902–910** set up the memory data channel transfer using PCI bus cycles and then perform the transfer on the data channel. Thus, in one embodiment, each multimedia device uses the PCI bus address and control signals to set up a date transfer on the respective memory data channel as discussed with reference to FIG. **3**A. A multimedia device may also use the PCI bus address and control signals to set up periodic transfers on the respective memory data channel. Thus, in a similar manner to that discussed above with respect to FIG. **3***d*, once the device has set up the periodic transfer, the memory **110** periodically transfers data to the multimedia devices, or vice versa, at periodic intervals.

In the embodiment of FIG. **19**, arbitration logic **936** is comprised in the chipset **106** and/or in the memory controller **934** and coupled to the memory controller **934**. The arbitration logic **936** receives memory requests from each of the devices **902–910** and performs arbitration for the devices **902–910** attempting to access the main memory **110**. In this embodiment, the multimedia devices **902–910** provide request signals on their respective channel to the arbitration logic **936**, and the arbitration logic **936** grants main memory access according to a desired arbitration method. The memory controller **934** also routes data transfers from the main memory **110** to the respective memory data channels.

FIG. **20**—Multimedia Devices

Referring now to FIG. **20**, a block diagram is shown illustrating one of the multimedia devices **902–910**, such as multimedia device **902**. As shown, the multimedia device **902** includes interface logic **940** comprising PCI interface circuitry **942** for communicating on the PCI bus **120**, and also including memory data channel interface logic **944** for interfacing to the respective data channel. The multimedia device **902** also may include a digital signal processor (DSP) **210** or other hardware circuitry for implementing a multimedia or communications function. Each of the multimedia devices **902–910** preferably includes the interface logic **940**, as shown in FIG. **20**.

The multimedia devices **902–910** preferably use their respective memory data channel only for high speed data transfers of real-time stream data information and/or periodic data transfers to or from the main memory **110**. In an alternate embodiment, the memory data channels are used by each multimedia device for any of various types of multimedia or communications data transfers to or from main memory **110**.

In one embodiment, each memory data channel includes only data lines, such as an 8 bit or 16 bit data path, and does not include address or control portions. In this embodiment of the invention, as mentioned above, each of the multimedia devices **902–910** uses the PCI bus **120** for addressing and control for transfers on the respective memory data channel.

FIG. **21**—PCI Bus Including a Real-Time Mode

Referring now to FIG. **21**, a computer system is shown which includes an expansion bus, preferably a PCI bus **120**, and which includes mode logic which selects between different modes of the PCI bus **120**. The computer system of FIG. **21** is similar to the computer system of FIG. **1**. However, the mode logic in the computer system of FIG. **21** is operable to place the PCI bus **120** in either a normal PCI mode or in a real-time /multimedia mode optimized for multimedia transfers of periodic data. As described below, multimedia devices use the PCI bus **120** for normal PCI transfers and also use the PCI bus lines in the multimedia mode for high speed data multimedia transfers, preferably transfers of periodic multimedia data. In the following description, elements which are preferably identical to elements previously described include the same reference numerals for convenience.

As shown, the computer system includes a central processing unit (CPU) **102** which is coupled through a CPU local bus **104** to a host/PCI/cache bridge or chipset **106**. The